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U.S. PATENT DOCUMENTS

Exam Init	Ref	Document Number	Issue Date	Name	Class	Sub Class
DWO		6,471,115 B1	10/29/2002	Ijuin et al.		
DWO		6,495,397 B2	12/17/2002	Kubota et al.		

FOREIGN PATENT DOCUMENTS

Exam Init	Ref	Document Number	Publication Date	Country	Name

OTHER DOCUMENTS

Exam Init	Ref	Author, Title, Date, Pertinent Pages, Etc.)
DWO		Klink et al., "Innovative Packaging Concepts for Ultra Thin Integrated Circuits," *IEEE 2001 Electronic Components and Technology Conference,* 5 pages (2001).
DWO		Dodd et al., "Impact of Substrate Thickness on Single-Event Effects in Integrated Circuits," *IEEE Transactions on Nuclear Science,* Vol. 48, No. 6, p. 1865-1871 (December 2001).
DWO		Sunohara et al., "Development of Wafer Thinning and Double-Sided Bumping Technologies for the Three-Dimensional Stacked LSI," *IEEE 2002 Electronic Components and Technology Conference,* p. 238-245 (2002).
DWO		http://www.webelements.com/webelements/elements/text/Au/enth.html, *Mark Winter, The University of Sheffield,* 4 pages (3/6/2003).
		"Some Practical Suggestions for Solder Preform Design," *Indium Corporation of America,* 1 page (prior to 5/12/03).
		"Mechanical Enabling for the Intel® Pentium® 4 Processor in the 478-Pin Package," *Intel Corporation* (October 2001).

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